



## Second Call for Papers

2026 International Conference on Simulation of  
Semiconductor Processes and Devices

# SISPAD2026

September 28 – 30, 2026

(Workshop: September 27)

Kumamoto-jo Hall, Kumamoto, JAPAN

### Organization:

#### Steering Chair:

Nobuya Mori (The Univ. of Osaka)

#### Conference Chair:

Hideki Minari (Sony)

#### Program Chair:

Hajime Tanaka (Kwansei Gakuin Univ.)

#### Program Vice-Chair:

Kai Tak Lam (TSMC)

Shingo Sato (Kansai Univ.)

#### Workshop:

Mincheol Shin (KAIST)

Yoon-Suk Kim (Samsung)

Hiroki Tokuhira (Kioxia)

Ken Uchida (The Univ. of Tokyo)

#### Local Arrangements:

Shunsuke Koba (Kobe City Col. Tech.)

Tomoya Nishimura (Renesas)

Shotaro Nishiura (Sony)

#### Publication:

Satofumi Souma (Kobe Univ.)

#### General Affairs:

Nobutoshi Aoki (Kumamoto Univ.)

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Yusuke Noda (Kyushu Inst. Tech.)

Yuki Ohuchi (Fuji Electric)

Mitsuhiro Sengoku (Toshiba)

Kenichiro Sonoda (Renesas)

Sponsored by The Japan Society of Applied Physics

Technical Co-sponsored by The IEEE Electron Devices Society



### Scope:

This conference provides an opportunity for the presentation and discussion of the latest advances in modeling and simulation of semiconductor devices and processes.

### Topics:

- Modeling and simulation of established semiconductor devices, including FinFETs, GAA FETs, ultra-thin SOI devices, TFTs, optoelectronic devices, memories, sensors, power electronic devices, and organic electronic devices
- Modeling and simulation of emerging devices including tunnel FETs, SETs, spintronic devices, straintronic devices, bio-electronic devices, cryogenic CMOS, emerging memories, neuromorphic devices, quantum computing devices, and new material-based devices for various applications
- Modeling and simulation of all sorts of semiconductor processes, including first-principles material design and growth simulation of nano-scale fabrication
- Fundamental aspects of device modeling and simulation, including quantum transport, thermal transport, fluctuation, noise, and reliability
- Compact modeling for circuit simulation, including low-power, high-frequency, and power electronics applications
- Process/device/circuit co-simulation in the context of system design and verification, including for emerging devices
- Modeling and simulation of interconnects, including noise, parasitic effects, and applications for advanced packaging schemes
- Modeling and simulation of equipment, topography, and lithography
- Numerical methods and algorithms, including grid generation, user interface, and visualization
- Enhancement of simulation methodologies, including multi-physics simulation, multi-scale approaches, and the use of artificial intelligence and quantum computing

### Abstract Submission:

Authors are invited to submit a two-page abstract (A4 or US Letter) including figures. Full submission information will be updated in the Second Call for Papers and the following website:

<https://sispad2026.jp/> (QR code on the right)



**Deadline for submission of abstracts: April 22, 2026**  
**(Extended)**

Authors of accepted papers will be required to submit a camera-ready four-page manuscript for inclusion in the Conference Proceedings.

### For inquiries, please contact:

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